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10/714,069	11/14/2003	Ramanand Venkata	000174-0284-101/A01084	2628

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EXAMINER	
BOLOURCHI, NADER	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,069	VENKATA ET AL.	
	Examiner	Art Unit	
	Nader Bolourchi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-41,47-51 and 57-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-41,47-51 and 57-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Restriction election

1. Applicant is kindly requested to cancel the unelected claims 1-24, 42-46, and 52-56 in response to this office action.

Drawings

2. The drawings are objected to because the rectangular boxes (250 and 294) shown in the drawing (Fig. 2) should be provided with descriptive text. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 26 is objected to because of the following informalities: replace "the predetermined rate" by the phrase - - a predetermined rate - - .

Appropriate correction is required.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 33 and 35 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 33 recites "the common signal **coming from** the reference clock signal" (lines 6-7). Claim 35 recites "a signal coming from the reference clock signal" (lines 4-5); which term "coming from" makes them vague and unclear. It is not clear what term "coming from" is referring to. Does it mean the common signal is the same as reference clock signal? Does it mean that there is a relationship between their frequencies?

Claim 34 and 36 are rejected due to its dependency to rejected claims 33 and 35, respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25-31, 33-34, 37-39, 41, 47-48, 50-51, 57-58, and 60-61 rejected under 35 U.S.C. 102(b) as being anticipated by Aunt et al. (US 2001/0033188 A1).

Regarding Claim 25, Aunt et al. ("Aunt" hereinafter) discloses an apparatus for receiving and unpadding padded blocks of data (Fig. 1) comprising: means for deriving from a single reference clock signal (the clock frequency of the CDR data signal shown as input of 22 from 30 in Fig. 1, i.e., the clock frequency embedded in the CDR as described in par. 36) first (the frequency of the reference clock signal shown as

REFCLK output of 42 in Fig. 1; par. 8) and second further clock signals (CLK input to 70 in Fig. 1; par. 8) having respective, different, first and second frequencies (RFCLK is different from eight CLK at the output of 130 in Fig. 2, and as described in pars. 44 and 45, CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36) , the first frequency being suitable for use of the first further clock signal in at least some processing of the padded blocks (Fig. 1: 50; padding is the serial "header" preceding serial "packet" is in par. 3), and the second frequency being suitable for use of the second further clock signal in at least some processing of the unpadded blocks (Fig. 1: 70 and 80; par. 41, where, DATA is unpadded block).

Regarding Claim 26, Aunt discloses as stated in rejection of claim 25 above. He further discloses that the padded blocks are received by the apparatus one after another at the predetermined rate, each padded block being received serially (data received serially as described in pars. 60 and 61, and wherein the apparatus further comprises: means for outputting unpadded blocks at the predetermined rate. (predetermined rate is caused by selectable value of J from 1 to 20 described in par. 60, and shown in Fig. 5: 220)

Regarding Claim 27, Aunt discloses as stated in rejection of claim 26 above. He further discloses means for registering each successive padded block (Fig. 5: 200; par. 60).

Regarding Claim 28, Aunt discloses as stated in rejection of claim 27 above. He further discloses that the means for registering is at least partly controlled by the first further

clock signal (REFCLK is used to generate eight CLK. At the out put of 130 as shown in Fig. 2; pars. 44 and 45)

Regarding Claim 29, Aunt discloses as stated in rejection of claim 28 above. He further discloses means for removing padding from each padded block registered by the means for registering to produce a corresponding unpadded block (Fig. 5: 70; par. 63).

Regarding Claim 30, Aunt discloses as stated in rejection of claim 29 above. He further discloses means for converting each unpadded block to a plurality of successive sub-blocks (Fig. 6; successive sub-blocks are successive parallel data word stored in RAM array 250 as described in par. 63).

Regarding Claim 31, Aunt discloses as stated in rejection of claim 30 above. He further discloses that the means for converting is at least partly controlled by the second further clock signal (CLK/J as described in par. 63).

Regarding Claim 33, Aunt discloses as stated in rejection of claim 25 above. He further discloses that the means for deriving comprises: first frequency dividing circuitry for dividing frequency of a common signal (REFCLK in Fig. 1) by a first division factor (W= 0.5 in REFCLK * W = EMBCLK as described in pars 36 and 37) to produce the second further clock signal, the common signal coming from the reference clock signal.

Regarding Claim 34, Aunt discloses as stated in rejection of claim 33 above. He further discloses that the means for deriving further comprises: second frequency dividing circuitry for dividing the frequency of the common signal by a second division factor (W=1 in REFCLK * W = EMBCLK as described in pars 36 and 37) to produce the first further clock signal.

Regarding Claim 37, Aunt discloses as stated in rejection of claim 34 above. He further discloses that the reference clock signal has a reference frequency having an integer-based relationship to the predetermined rate (The frequency of the reference clock signal REFCLK has a known relationship to the clock frequency of the CDR data signal as recited in par. 8; REFCLK has a known relation to CLK which has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36, which is related to predetermined rate, caused by selectable value of J from 1 to 20 described in par. 60, and shown in Fig. 5: 220).

Regarding Claim 38, Aunt discloses as stated in rejection of claim 37 above. He further discloses that the means for deriving comprises: means for performing integer-based manipulation of the reference frequency (Fig. 1: 40) to produce the first and second further clock signals.

Regarding Claim 39, Aunt discloses as stated in rejection of claim 38 above. He further discloses that the means for performing comprises: first means (Fig. 1: 22; par. 36) for

performing first integer-based manipulation of the reference frequency to produce a common signal (Fig. 1: 22; par. 36); and second means (Fig. 1: 40) for performing second integer-based frequency manipulation of the common signal to produce the second further clock signal

Regarding Claim 40, Aunt discloses as stated in rejection of claim 39 above. He further discloses that the means for performing further comprises: third means for performing third integer-based frequency manipulation of the common signal to produce the first further clock signal (Fig. 1: 42 in 40).

Regarding Claim 41, Aunt discloses as stated in rejection of claim 25 above. He further discloses byte alignment circuitry for using the padding of the padded blocks to locate data block boundaries (Fig. 5; pars. 60-62).

Regarding Claim 47, Aunt discloses a method of receiving and unpadding padded blocks of data (Fig. 1) comprising deriving from a reference clock signal (the clock frequency of the CDR data signal shown as input of 22 from 30 in Fig. 1, i.e., the clock frequency embedded in the CDR as described in par. 36) a common signal (input of 24 in Fig. 1); producing first (the frequency of the reference clock signal shown as REFCLK output of 42 in Fig. 1; par. 8) and second further clock signals from the common signal (CLK input to 70 in Fig. 1; par. 8); using the first further clock signal in at least some processing of the padded data (Fig. 1: 50; padding is the serial "header"

preceding serial "packet" is in par. 3); and using the second further clock signal in at least some processing of the unpadded data (Fig. 1: 70 and 80; par. 41, where, DATA is unpadded block), wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal (RFCLK is different from eight CLK at the output of 130 in Fig. 2, and as described in pars. 44 and 45, CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36).

Regarding Claim 48, Aunt discloses as stated in rejection of claim 47 above. He further discloses that the common signal frequency is different from frequency of the reference signal (Fig. 1: output of 30, is different from input of 50)

Regarding Claim 50, Aunt discloses as stated in rejection of claim 47 above. He further discloses that the deriving comprises: using integer-based frequency manipulation of the reference clock signal to produce the common signal (Fig.1, 22; par. 36).

Regarding Claim 51, Aunt discloses as stated in rejection of claim 47 above. He further discloses using integer-based frequency manipulation of the common signal to produce second further clock signals (CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36).

Regarding Claim 57 , Aunt discloses an apparatus for receiving and unpadding padded blocks (Fig. 1) of data comprising: first circuitry (Fig. 1: 22) adapted to derive from a reference clock signal (the clock frequency of the CDR data signal shown as input of 22 from 30 in Fig. 1, i.e., the clock frequency embedded in the CDR as described in par. 36) a common signal (input of 24 in Fig. 1); second circuitry (Fig. 1: 40) adapted to produce first (the frequency of the reference clock signal shown as REFCLK output of 42 in Fig. 1; par. 8) and second further clock signals from the common signal (CLK input to 70 in Fig. 1; par. 8) ; third circuitry adapted to use the first further clock signal in at least some processing of the padded data (Fig. 1: 50; padding is the serial "header" preceding serial "packet" is in par. 3); and fourth circuitry adapted to use the second further clock signal in at least some processing of the unpadded data (Fig. 1: 70 and 80; par. 41, where, DATA is unpadded block), wherein the first and second further clock signals have respective, different, first and second frequencies, at least one of which is different from frequency of the common signal (RFCLK is different from eight CLK at the output of 130 in Fig. 2, and as described in pars. 44 and 45, CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36).

Regarding Claim 58, Aunt discloses as stated in rejection of claim 57 above. He further discloses that the common signal frequency is different from frequency of the reference clock signal (Fig. 1: output of 30, is different from input of 50).

Regarding Claim 60, Aunt discloses as stated in rejection of claim 57 above. He further discloses that the first circuitry comprises: circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal (par. 36).

Regarding Claim 61, Aunt discloses as stated in rejection of claim 57 above. He further discloses that the second circuitry comprises: circuitry for performing integer-based frequency manipulation of the reference clock signal to produce the common signal (Fig. 1: 42 which included in circuitry 40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention

was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 32, 49, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aunt et al.

Regarding Claim 32, Aunt discloses as stated in rejection of claim 25above. He is silent about number of bits in each padded block (number of header bit discussed in par. 3 is not explicitly disclosed). Furthermore, he uses J from 1 to 20 as number of bits in data sub-blocks.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have 66 bits of padded data, and each unpadded block consists of 64 bits of data because, Applicant has not disclosed that 66 bits of padded data, and each unpadded block consists of 64 bits of data provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any number of "header" and 20 bits in a sub-block of unpadded data because clock data recovery (CDR) perform well. Therefore, it would have been an obvious matter of design choice to modify Aunt et al. to obtain the invention as specified in claim.

Regarding Claim 49, Aunt discloses as stated in rejection of claim 47 above. He further discloses that second frequencies is different from the common signal frequency (RFCLK is different from eight CLK at the output of 130 in Fig. 2, and as described in pars. 44 and 45, CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36). But he is silent about the differences with first frequency.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have first frequency to be different from the common frequency by means of a divider or scalar as it is used by Aunt because. Therefore, it would have been an obvious matter of design choice to modify Aunt et al. to obtain the invention as specified in claim.

Regarding Claim 59, Aunt discloses as stated in rejection of claim 57 above. He further discloses that second frequencies is different from the common signal frequency (RFCLK is different from eight CLK at the output of 130 in Fig. 2, and as described in pars. 44 and 45, CLK has same frequency as EMBCLK, where REFCLK * W = EMBCLK as shown in par. 36). But he is silent about the differences with first frequency.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have first frequency to be different from the common frequency by means of a divider or scalar as it is used

by Aunt because. Therefore, it would have been an obvious matter of design choice to modify Aunt et al. to obtain the invention as specified in claim.

Remarks

8. No claim is allowed.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Franaszek et al (US 4,486,739 A); Feuerstraeter et al. (US 2003/0058894 A1);

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nader Bolourchi whose telephone number is (571) 272-8064. The examiner can normally be reached on M-F 8:30 to 4:30.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David. C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Nader Bolourchi

Date 1/4/2008

David Payne

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER